REMARKS

Claims 1-3, 5, and 21-32 are presented for further examination. Claims 1-3 have been amended. Claims 21-32 are new.

In the Office Action mailed December 8, 2009, the Examiner rejected claim 2 under 35 U.S.C. § 112, as indefinite because the recitation of the first value in claim 1 was inconsistent with that of claim 2. Claims 1, 4-8, 10-13, and 15-20 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent Publication No. 2002/0097812 ("Wiss"). Claim 2 is rejected as obvious over Wiss in view of U.S. Patent No. 6,289,048 ("Richards et al."). Claim 14 was rejected as obvious over Wiss in view of U.S. Patent No. 6,442,217 ("Cochran").

Applicant respectfully requests reconsideration and further examination of the claims.

Section 112 Rejection

Claims 1 and 2 have been amended in a manner that renders moot the rejection under Section 112 inasmuch as the "first signal" is no longer recited in these claims.

Claim Rejections

Independent claim 1 and new independent claims 22 and 26 are directed, respectively, to the embodiments set forth in Figures 1-3.

The embodiment of Figure 1, which is captured in claims 1-3, 5, and new dependent claim 22, has a first circuit that receives the uncompensated I and Q components from the demodulated input signal and cross correlates these two signals through a first multiplier, and generates the square of each signal through second and third multipliers, and then divides the output of the first and second multipliers and divides the output of the second and third multipliers, with the output of both dividers input to a phase gain compensator that generates the compensated I and Q signals. The function of the circuit of Figure 1 is recited in claim 1 as well as dependent claims 2, 3, and 5, and the structure of Figure 1 is recited more particularly in claim 22. The function and structure of the circuit of Figure 1 is not found in any of the references cited by the Examiner, taken alone or in any combination thereof. Thus, claim 1 as well as

dependent claims 2, 3, 5, and 22 are allowable over the references cited and applied by the Examiner.

New claim 22 recites the first circuit receiving as inputs the output of the phase gain compensation circuit, thus receiving the compensated I and Q signals. These two signals are multiplied or cross correlated through a first multiplier and the compensated I signal is squared through a second multiplier and then the output of the first multiplier is divided by the output of the second multiplier and the integral is taken through an integrator (25). The output of the integrator is received as an input to the phase gain compensation circuit 17 along with the uncompensated I and Q signals. The function of the circuit of Figure 2 is recited in claim 22, and the structure of this circuit is recited more particularly in claim 26. None of the references cited and applied by the Examiner, taken alone or in any combination thereof, teach or suggest the circuit of Figure 2 as found in claims 22-26.

Claims 27-32 are directed to the embodiment illustrated in Figure 3 in which the first circuit squares the compensated I and Q components through respective multipliers and a subtractor takes the difference of the output of the two multipliers, which output then passes through an integration circuit that generates an integration signal, which is received at an input to the phase gain compensation circuit. None of the references cited and applied by the Examiner, taken alone or in any combination thereof, teach or suggest this circuit.

In view of the foregoing, applicant respectfully submits that claims 1-3, 5, and 21-32 are in condition for allowance. In the event the Examiner finds minor informalities that can be resolved by telephone conference, the Examiner is urged to contact the undersigned by telephone at (206) 622-4900 in order to expeditiously resolve prosecution of this application. Consequently, early and favorable action allowing these claims and passing this case to issuance is respectfully solicited.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC

/E. Russell Tarleton/
E. Russell Tarleton
Registration No. 31,800

ERT:alb

701 Fifth Avenue, Suite 5400
Seattle, Washington 98104
Phone: (206) 622-4900
Fax: (206) 682-6031

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